What is claimed is:

1. A branch target prefetch apparatus comprising:

a presbyopic target buffer configured to receive a presbyopic target buffer record, wherein the presbyopic target buffer record maps an entry location of a first code region to an entry location of a second code region; and

a prefetch stream buffer configured to receive instructions from the second code region responsive to an instruction pointer encountering the entry location of the first code region.

2. The branch target prefetch apparatus of claim 1 wherein the presbyopic target buffer is configured to receive the presbyopic target buffer record responsive to a branch instruction being encountered in the first code region, the branch instruction having a branch target address equal to the entry location of the second code region.

3. The branch target prefetch apparatus of claim 2 further comprising a branch target buffer configured to receive a branch target buffer record that maps an address of the branch instruction to the entry location of the second code region.

4. The branch target prefetch apparatus of claim 3 wherein the presbyopic target buffer is configured to receive a plurality of presbyopic target buffer records, and is further configured to be searched recursively.

5. The branch target prefetch apparatus of claim 4 wherein the prefetch stream buffer is configured to receive instructions from a plurality of code regions responsive to a recursive search of the presbyopic target buffer.

6. The branch target prefetch apparatus of claim 5 wherein the prefetch stream buffer is configured to differentiate between instructions such that instructions from different ones of the plurality of code regions can be invalidated.

7. The branch target prefetch apparatus of claim 3 wherein the branch target buffer record includes a first confidence counter having a first number of bits, and the presbyopic target buffer record includes a second confidence counter having a second number of bits that is greater than the first number of bits.

8. The branch target prefetch apparatus of claim 1 wherein the presbyopic target buffer record is configured to map the entry location of the first code region to entry locations of a plurality of second code regions.

9. The branch target prefetch apparatus of claim 1 wherein a cache memory has a cache latency associated therewith, and the prefetch target buffer has a depth at least as deep as one cache latency.

10. A processor comprising:

a branch target buffer responsive to fetched instruction addresses, wherein the branch target buffer is configured to map branch instruction addresses to branch target addresses; and

a presbyopic target buffer responsive to the branch target buffer, wherein the presbyopic target buffer is configured to map branch target addresses to subsequent branch target addresses.

11. The processor of claim 10 further comprising:

a stream buffer configured to receive instructions fetched from subsequent branch target addresses specified in the presbyopic target buffer.

12. The processor of claim 10 wherein the presbyopic target buffer is configured to be recursively searched to predict a plurality of subsequent branch target addresses.

13. The processor of claim 10 wherein the presbyopic target buffer implements skip-adjacent mapping.

14. The processor of claim 10 wherein a complete branch target address is specified by a fixed number of bits, and the presbyopic target buffer includes mapping records that specify branch target addresses using less than the fixed number of bits.

15. A processor comprising:

a branch target buffer responsive to fetched instruction addresses, wherein the branch target buffer is configured to be searched for the fetched instruction addresses and corresponding branch target addresses;

a presbyopic target buffer responsive to the branch target buffer, wherein the presbyopic target buffer is configured to be searched for subsequent dynamic blocks as a function of branch target addresses.

16. The processor of claim 15 wherein the presbyopic target buffer is configured to map branch target addresses to subsequent dynamic block exit addresses.

17. The processor of claim 16 wherein the branch target buffer is further responsive to subsequent dynamic block exit addresses from the presbyopic target buffer.

18. The processor of claim 17 wherein the branch target buffer and presbyopic target buffer are configured to be searched recursively in combination.

19. A processor comprising:

a first fetch buffer configured to receive instructions prefetched from predicted branch target addresses; and

a second fetch buffer configured to receive instructions prefetched from predicted subsequent blocks.

20. The processor of claim 19 wherein the second fetch buffer includes a coloring field for each instruction included therein, such that each instruction included therein can be assigned a color.

21. The processor of claim 19 wherein the second fetch buffer includes a subsequent block demarcation mechanism to distinguish prefetched instructions from different predicted subsequent blocks.

22. The processor of claim 19 further including a branch target buffer having records that when populated, map branches to predicted branch targets.

23. The processor of claim 22 further including a presbyopic target buffer having records that when populated, map predicted branch target addresses to predicted subsequent blocks.

24. The processor of claim 23 wherein the presbyopic target buffer maps each predicted branch target address to a plurality of predicted subsequent blocks.

25. The processor of claim 23 wherein the presbyopic target buffer is configured to be recursively searched.

26. An instruction prefetch method comprising:

in a first buffer that maps branch instruction addresses to block entry addresses, searching for a first buffer record having a branch instruction address that matches a current instruction address;

when the first buffer record is found, searching a second buffer that maps block entry addresses to subsequent block entry addresses for a second buffer record having a block entry address matching the first buffer record; and

when the second buffer record is found, prefetching instructions beginning at a subsequent block entry address included in the second buffer record.

27. The method of claim 26 wherein prefetching comprises entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered.

28. The method of claim 26 further comprising:

searching the second buffer recursively; and

for each matching record found in the second buffer, each matching record having a corresponding subsequent block entry address, prefetching instructions from each of the corresponding subsequent block entry addresses.

29. The method of claim 28 wherein prefetching comprises:

entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered; and

assigning a different color to instructions fetched from different subsequent block entry addresses.

30. The method of claim 29 wherein each recursive search represents a predicted branch, the method further comprising flushing from the stream buffer instructions prefetched as a result of a mispredicted branch.